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| 10/092,255 | 03/07/2002 | Yoshinori Ogawa | 1248-0583P | 9284 |

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| EXAMINER | |
|---|---|
| SHAPIRO, LEONID | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2673 | |

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/092,255 | OGAWA ET AL. | |
| | Examiner | Art Unit | |
| | Leonid Shapiro | 2673 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,12 and 14* is/are rejected.

7)☒ Claim(s) *11, 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 3, 12, 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoneda et al. (US Patent No. 5,926,158).

As to claim 1, Yoneda et al. teaches an image display device (See Col. 1, Lines 8-10), comprising:

a plurality of scanning signal lines (See Fig. 23, items 102) and a plurality of data lines which crossing each other (See Fig. 123, items 101, Col. 1, Lines 13-20) an electro-optical element (See Fig. 23, item Cp), and a switching element (See Fig. 23, item TR) and a pixel capacitor (See Fig. 23, item Cs) being provided in each pixel region (See Fig. 23, items Z , Col. 1, Lines 21-32) surrounded by adjacent two of plurality of scanning lines (See Fig. 23, items 102, Col. 1, Lines 18-20) and adjacent two of plurality of data signal lines (See Fig. 23, items 102, Col. 1, Lines 18-20);

a data signal driving circuit for outputting voltages for display in mutually reverse polarities with respect to a pair of adjacent pixels in direction of the data signal lines (See Figs. 12, items m – m+3, n - n+1, Col. 14, Lines 36-62); and

short-circuit means for short-circuiting respective pixel capacitors of pair of adjacent pixels (See Fig. 16, items P11-P12, SW12, Col. 15, Lines 38-51) before

applying the voltages for display to a pixel to be scanned first of the pair of adjacent pixels in the direction of the data signal lines when scanning (See Fig. 16, items Xm+1-Xm+3, P11-P12, SW12, Col. 15, Lines 51-58) in switching polarities for display (See Figs. 12, items m – m+3, n - n+1, Col. 14, Lines 36-62).

As to claim 3, Yoneda et al. teaches data signal line driving circuit outputs voltages for gradation display in mutually reverse polarities with respect to a pair pixels adjacent in a data signal lines display (See Figs. 12, items m – m+3, n - n+1, Col. 14, Lines 36-62).

As to claim 12, Yoneda et al. teaches an image display device (See Col. 1, Lines 8-10), comprising:

a plurality of scanning signal lines (See Fig. 23, items 102) and a plurality of data lines which crossing each other (See Fig. 123, items 101, Col. 1, Lines 13-20);

an electro-optical element (See Fig. 23, item Cp), and a switching element (See Fig. 23, item TR) and a pixel capacitor (See Fig. 23, item Cs) being provided in each pixel region (See Fig. 23, items Z , Col. 1, Lines 21-32) surrounded by adjacent two of plurality of scanning lines (See Fig. 23, items 102, Col. 1, Lines 18-20) and adjacent two of plurality of data signal lines (See Fig. 23, items 102, Col. 1, Lines 18-20);

a data signal driving circuit for outputting voltages for display in mutually reverse polarities with respect to a pair of adjacent pixels in direction of the data signal lines (See Figs. 12, items m – m+3, n - n+1, Col. 14, Lines 36-62); and

scanning signal line driving circuit carries out a selection scanning (See Fig. 16, items P11-P12, SW12, Col. 15, Lines 38-51) with respect to a scanning signal line of the pixel to be scanned first together with a scanning signal line of the pixel to be scanned next of a pair of adjacent pixels in the direction of data signal lines (See Fig. 16, items Xm+1-Xm+3, P11-P12, SW12, Col. 15, Lines 51-58) before applying the voltages for display to the pixel to be scanned first of pair of adjacent pixels when scanning in switching polarities of the voltages for display (See Figs. 18-19, items LWP1-LWP2, Col. 16, Lines 5-65).

As to claim 14, Yoneda et al. teaches an image display device (See Col. 1, Lines 8-10), comprising:

a plurality of scanning signal lines (See Fig. 23, items 102) and a plurality of data lines which crossing each other (See Fig. 123, items 101, Col. 1, Lines 13-20);

an electro-optical element (See Fig. 23, item Cp), and a switching element (See Fig. 23, item TR) and a pixel capacitor (See Fig. 23, item Cs) being provided in each pixel region (See Fig. 23, items Z , Col. 1, Lines 21-32) surrounded by adjacent two of plurality of scanning lines (See Fig. 23, items 102, Col. 1, Lines 18-20) and adjacent two of plurality of data signal lines (See Fig. 23, items 102, Col. 1, Lines 18-20);

a data signal driving circuit for outputting voltages for display in mutually reverse polarities with respect to a pair of adjacent pixels in direction of the data signal lines (See Figs. 12, items m – m+3, n - n+1, Col. 14, Lines 36-62); and

short-circuit means for short-circuiting respective pixel capacitors in the liquid crystal panel of pair of adjacent pixels (See Fig. 16, items P11-P12, SW12, Col. 15, Lines 38-51) in a non-selection period directly before a selection-scanning period of a target scanning signal line when scanning (See Fig. 16, items Xm+1-Xm+3, P11-P12, SW12, Col. 15, Lines 51-58) by switching polarities for gradation display (See Figs. 12, items m – m+3, n - n+1, Col. 14, Lines 36-62).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2, 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda et al. as applied to claim 1 above, and further in view of Udo et al. (Pub.: US 2002/0050972 A1).

As to claims 2, 6, Yoneda et al. does not teach data signal line driving circuit outputs voltages for gradation display in mutually reverse polarities with respect to a pair pixels adjacent in a direction of scanning signal lines and frames.

Udo et al. teaches data signal line driving circuit outputs voltages for gradation display in mutually reverse polarities with respect to a pair pixels adjacent in a direction of scanning signal lines and frames (See Figs. 2A-2B, page 2, paragraph 0040).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Udo et al. into Yoneda et al. system in order to reduce power consumption (See page 1, paragraph 0012 in the Udo et al. reference).

As to claim 4, Yoneda et al. does not teach a positive voltage output section for outputting a positive voltage converted from a data signal; and a negative voltage output section for outputting a negative voltage converted from a data signal; a switching section for switching positive output section and negative output section between adjacent data signal lines; wherein positive voltage output section negative voltage output section are used in common in adjacent data signal lines.

Udo et al. teaches a positive voltage output section for outputting a positive voltage converted from a data signal (See Fig. 4, item PS1, page 3, paragraph 0054); and a negative voltage output section for outputting a negative voltage converted from a data signal (See Fig. 4, item NS1, page 3, paragraph 0054); a switching section for switching positive output section and negative output section between data signal lines (See Fig. 4, items P1-P2, N1-N2, page 3, paragraph 0055); wherein positive voltage output section negative voltage output section are used in common in data signal lines; adjacent signal lines (See Fig. 9, items D1-D2, S1, page 1, paragraph 0010).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Udo et al. into Yoneda et al. system in order to reduce power consumption (See page 1, paragraph 0012 in the Udo et al. reference).

As to claim 5, Yoneda et al. does not show positive voltage output section includes a positive polarity D/A converter and operational amplifier of N-channel MOS

transistor input; and negative voltage output section includes a negative polarity D/A converter and operational amplifier of P-channel MOS transistor input.

Udo et al. teaches each of transfer gates has a PMOS and NMOS transistors connected in parallel to each other (See Figs. 5-6, items 21-22, page 3, 0057-0058).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Udo et al. into Yoneda et al. system in order to reduce power consumption (See page 1, paragraph 0012 in the Udo et al. reference).

3. Claim 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Udo et al. in view of Masami et al. (JP 09-212137).

As to claim 7, Yoneda et al. teaches an image display device (See Col. 1, Lines 8-10), comprising:

a plurality of scanning signal lines (See Fig. 23, items 102) and a plurality of data lines which crossing each other (See Fig. 123, items 101, Col. 1, Lines 13-20);

an electro-optical element (See Fig. 23, item Cp), and a switching element (See Fig. 23, item TR) and a pixel capacitor (See Fig. 23, item Cs) being provided in each pixel region (See Fig. 23, items Z , Col. 1, Lines 21-32) surrounded by adjacent two of plurality of scanning lines (See Fig. 23, items 102, Col. 1, Lines 18-20) and adjacent two of plurality of data signal lines (See Fig. 23, items 102, Col. 1, Lines 18-20);

a data signal line driving circuit for outputting voltages for display in mutually reverse polarities with respect to a pair of adjacent pixels (See Figs. 12, items m – m+3, n - n+1, Col. 14, Lines 36-62);

wherein data signal line driving circuit outputs voltages for gradation display in mutually reverse polarities with respect to a pair of adjacent pixels in direction of data signal line (See Figs. 12, items m – m+3, n - n+1, Col. 14, Lines 36-62); and

scanning signal line driving circuit carries out a selection-scanning operation by switching polarities of voltages for gradation display (See Fig. 16, items P11-P12, SW12, Col. 15, Lines 38-51) with respect to both of a scanned signal line to be scanned first and a scanned signal line to be scanned next of a pair (See Fig. 16, items Xm+1-Xm+3, P11-P12, SW12, Col. 15, Lines 51-58) in a first half of the selection-scanning period of the scanning signal line to be scanned first of the pair (See Figs. 18-19, items LWP1-LWP2, Col. 16, Lines 5-65).

Yoneda et al. does not show separation means for separating an output stage of data signal line driving circuit from a data signal line in a first half of a selection-scanning period of each scanning signal line by a scanning line driving circuit, separation means being provided between output stage of data signal line driving circuit and data signal line.

Masami et al. teaches separation means for separating an output stage of data signal line driving circuit from a data signal line in a first half of a selection-scanning period of each scanning signal line by a scanning line driving circuit (See Figures 1-2, items t1-t2, 101-102, page 3, paragraph 0017), separation means being

provided between output stage of data signal line driving circuit and data signal line (See Figure 1, item 102).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Masami et al. into Yoneda et al. in order to reduce power consumption (See Problem to be solved in Masami et al. reference).

As to claim 8, Yoneda et al. teaches an image display device (See Col. 1, Lines 8-10), comprising:

a plurality of scanning signal lines (See Fig. 23, items 102) and a plurality of data lines which crossing each other (See Fig. 123, items 101, Col. 1, Lines 13-20);

an electro-optical element (See Fig. 23, item Cp), and a switching element (See Fig. 23, item TR) and a pixel capacitor (See Fig. 23, item Cs) being provided in each pixel region (See Fig. 23, items Z , Col. 1, Lines 21-32) surrounded by adjacent two of plurality of scanning lines (See Fig. 23, items 102, Col. 1, Lines 18-20) and adjacent two of plurality of data signal lines (See Fig. 23, items 102, Col. 1, Lines 18-20);

a data signal line driving circuit for outputting voltages for display in mutually reverse polarities with respect to a pair of adjacent pixels (See Figs. 12, items m – m+3, n - n+1, Col. 14, Lines 36-62);

wherein data signal line driving circuit outputs voltages for gradation display in mutually reverse polarities with respect to a pair of adjacent pixels in direction of data signal line (See Figs. 12, items m – m+3, n - n+1, Col. 14, Lines 36-62); and

scanning signal line driving circuit carries out a selection-scanning operation by switching polarities of voltages for gradation display (See Fig. 16, items P11-P12, SW12, Col. 15, Lines 38-51) with respect to both of a scanned signal line to be scanning first and a scanned signal line to be scanning next of a pair (See Fig. 16, items Xm+1-Xm+3, P11-P12, SW12, Col. 15, Lines 51-58).

Yoneda et al. does not show separation means for separating an output stage of data signal line driving circuit from a data signal line in a first half of a selection-scanning period of each scanning signal line by a scanning line driving circuit, separation means being provided between output stage of data signal line driving circuit and data signal line and the blanking period directly before the selection-scanning period of the scanning signal line to be scanned first of the pair.

Masami et al. teaches separation means for separating an output stage of data signal line driving circuit from a data signal line in a first half of a selection-scanning period of each scanning signal line by a scanning line driving circuit (See Figures 1-2, items t1-t2, 101-102, page 3, paragraph 0017), separation means being provided between output stage of data signal line driving circuit and data signal line (See Figure 1, item 102) and the blanking period directly before the selection-scanning period of the scanning signal line to be scanned first of the pair (See Fig. 1-2, items 101-102, page 2, paragraphs 0014, 0017).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Masami et al. into Yoneda et al. in order to reduce power consumption (See Problem to be solved in Masami et al. reference).

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda et al. and Masami et al. in view of Hayashi et al. (US Patent No. 6, 130, 654).

Masami et al. teaches control means for controlling to cut off separation means in a blanking period, blanking period being provided directly before selection-scanning period of the scanning signal line to be scanned first of the pair, and to perform the selection-scanning operation of the target pair of scanning signal lines in the cut-off state of separation means (See Fig. 1-2, items 101-102, page 2, paragraphs 0014, 0017).

Yoneda et al. and Masami et al. do not show blanking period at every two horizontal scanning periods.

Hayashi et al. teaches blanking period at every two horizontal scanning periods (See Fig. 8a, items 1H,Vp1, Col. 10, Lines 23-36).

It would have been obvious to one of ordinary skill in the art at the time of invention to use blanking period at every two horizontal scanning periods as shown by Hayashi et al. in Masami et al. and Yoneda et al. apparatus in order to display uniform brightness images (See Col. 1, Lines 44-47 in Hayashi et al. reference).

***Response to Amendment***

5. Applicant's arguments filed on 07.19.04 with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

***Allowable Subject Matter***

6. Claims 11, 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Relative to claim 11 the major difference between the teaching of the prior art of record (Yoneda et al. and Masami) and the instant invention is that the said prior art **does not teach** short-circuit means carries out selection scanning of respective scanning signal lines of the pair of adjacent pixels in the direction of the data signal lines at the **same** time to drive the switching elements of the pair of pixels.

Relative to claim 13 the major difference between the teaching of the prior art of record (Yoneda et al. and Masami) and the instant invention is that the said prior art **does not teach** scanning signal line driving circuit carries out selection scanning signal line of the pixel to be scanned first together with the scanning signal line of the pixel to be scanned next, separation means electrically separates the output stage of the data signal line driving circuit from the signal line.

***Telephone inquire***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ls 12.21.04

VIJAY SHANKAR
PRIMARY EXAMINER